

PRELIMINARY

PM100CLA120

FLAT-BASE TYPE
INSULATED PACKAGE

Notice : This is not a final specification. Some parametric limits are subject to change.

PM100CLA120

Pre.	T.Marumo	Rev.	A
Apr.	M.Yamamoto May 23,2003	<i>T. Marumo</i> <i>M. Yamamoto</i> July 14, 2003	

Feature

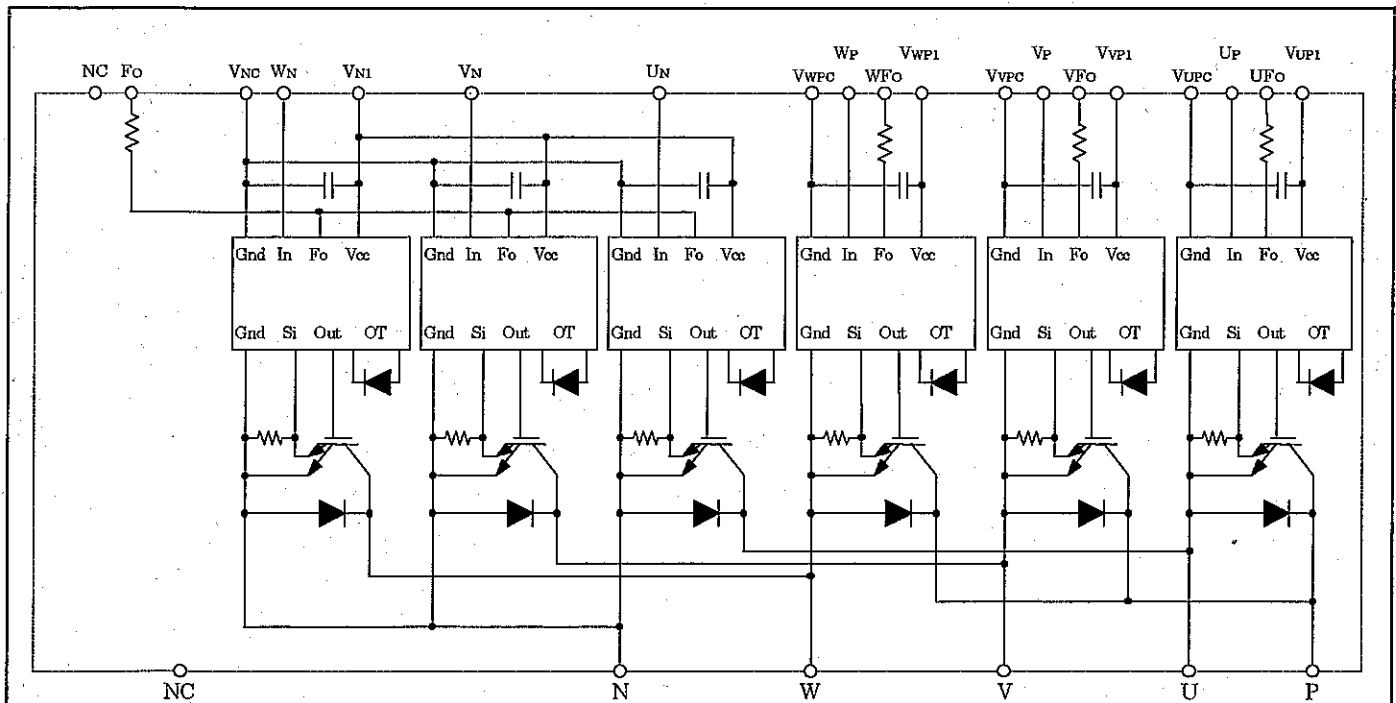
- a) Adopting new 5th generation IGBT(CSTBT) chip, which performance is improved by 1μm fine rule process.
For example, typical $V_{ce(sat)}=1.9V$ @ $T_j=125^{\circ}C$
- b) I adopt the over-temperature conservation by T_j detection of CSTBT chip, and error output is possible from all each conservation upper and lower arm of IPM.

- 3φ 100A, 1200V Current-sense IGBT type inverter
- Monolithic gate drive & protection logic
- Detection, protection & status indication circuits for, short-circuit, over-temperature & under-voltage (P-Fo available from upper arm devices)
- Acoustic noise-less 18.5kW/22kW class inverter application

OUTLINE DRAWING Dimensions in mm

See Page 7

APPLICATION : General purpose inverter, servo drives and other motor controls



Maximum Ratings ($T_j = 25^\circ\text{C}$, unless otherwise noted)

Inverter Part

Item	Symbol	Condition	Rating	Unit
Collector-Emitter Voltage	V_{CES}	$V_D = 15\text{V}, V_{CIN} = 15\text{V}$	1200	V
Collector Current	$\pm I_C$	$T_C = 25^\circ\text{C}$	100	A
Collector Current (Peak)	$\pm I_{CP}$	$T_C = 25^\circ\text{C}$	200	A
Collector Dissipation	P_C	$T_C = 25^\circ\text{C}$ (Note-1)	595	W
Junction Temperature	T_j		-20 ~ +150	$^\circ\text{C}$

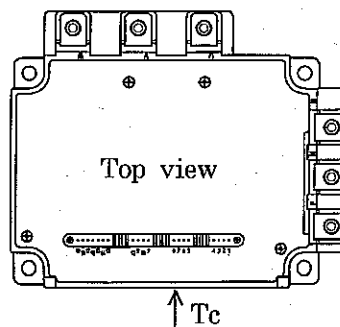
Control Part

Item	Symbol	Condition	Rating	Unit
Supply Voltage	V_D	Applied between : $V_{UP1}-V_{UPC}$ $V_{VP1}-V_{VPC}, V_{WP1}-V_{WPC}, V_{UN1}-V_{UNC}$	20	V
Input Voltage	V_{CIN}	Applied between : U_P-V_{UPC}, V_P-V_{VPC} $W_P-V_{WPC}, U_N \cdot V_N \cdot W_N - V_{NC}$	20	V
Fault Output Supply Voltage	V_{FO}	Applied between : $U_{FO}-V_{UPC}, V_{FO}-V_{VPC}$ $W_{FO}-V_{WPC}, F_O - V_{NC}$	20	V
Fault Output Current	I_{FO}	Sink current at $U_{FO}, V_{FO}, W_{FO}, F_O$ terminals	20	mA

Total System

Item	Symbol	Condition	Rating	Unit
Supply Voltage Protected by SC	$V_{CC(prot)}$	$V_D = 13.5 \sim 16.5\text{V}$ Inverter Part, $T_j = +125^\circ\text{C}$ Start	800	V
Supply Voltage (Surge)	$V_{CC(surge)}$	Applied between : P-N, Surge value	1000	V
Module Case Operating Temperature	T_C	(Note-1)	-20 ~ +100	$^\circ\text{C}$
Storage Temperature	T_{stg}		-40 ~ +125	$^\circ\text{C}$
Isolation Voltage	Viso	60Hz, Sinusoidal Charged part to Base, AC 1 min.	2500	Vrms

(Note-1) T_c (base plate) measurement point is below.



Thermal Resistances

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Junction to case Thermal Resistances	Rth(j-c)Q	Inverter IGBT part (per 1/6) (Note-2)	—	—	0.16*	°C/W
	Rth(j-c)F	Inverter FWDi part (per 1/6) (Note-2)	—	—	0.26*	
	Rth(j-c)Q	Inverter IGBT part (per 1/6) (Note-1)	—	—	0.21	
	Rth(j-c)F	Inverter FWDi part (per 1/6) (Note-1)	—	—	0.34	
Contact Thermal Resistance	Rth(c-f)	Case to fin, (per 1 module) Thermal grease applied (Note-1)	—	—	0.023	

(Note-2) Tc measurement point is just under the chip.

* If you use this value, Rth(f-a) should be measured just under the chips.

Electrical Characteristics (Tj = 25°C unless otherwise noted)

Inverter Part

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Collector-Emitter Saturation Voltage	VCE(sat)	VD = 15V, VCIN = 0V IC = 100A, Pulsed Fig.1	Tj = 25°C	—	1.9	—	V
			Tj = 125°C	—	1.9	—	
FWDi Forward Voltage	VEC	-IC = 100A, VCIN = 15V VD = 15V Fig.2	—	2.5	3.5	V	
Switching Time	ton	VD = 15V, VCIN = 0V ↔ 15V VCC = 600V, IC = 100A Tj = 125°C, Inductive Load Fig.3,4	—	0.5	1.0	2.5	μs
	trr		—	0.15	0.3		
	tc(on)		—	0.4	1.0		
	toff		—	2.0	3.0		
	tc(off)		—	0.7	1.2		
Collector-Emitter Cutoff Current	ICES	VCE = VCES VD = 15V Fig.5	Tj = 25°C	—	—	1	mA
			Tj = 125°C	—	—	10	

Control Part

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Circuit Current	ID	VD = 15V VCIN = 15V	VNI-VNC	—	18	28	mA
			VXPI-VXPC	—	6	12	
Input ON Threshold Voltage	Vth(ON)	Applied between : UP-VUPC, VP-VVPC	1.2	1.5	1.8	V	
Input OFF Threshold Voltage	Vth(OFF)	WP-VWPC, UN-VN-WN-VNC	1.7	2.0	2.3		
Short Circuit Trip Level	SC	-20 ≤ Tj ≤ 125°C VD = 15V Fig.3,6	200	—	—	A	
Short Circuit Current Delay Time	toff(SC)	VD = 15V Fig.3,6	—	0.2	—	μs	
Over Temperature Protection	OT	Detect Tj of IGBT chip	Trip level	135	145	155	°C
	OTr		Reset level	—	125	—	
Supply Circuit Under Voltage Protection	UV	-20 ≤ Tj ≤ 125°C	Trip level	11.5	12.0	12.5	V
	UVr		Reset level	—	12.5	—	
Fault Output Current	Ifo(H)	VD = 15V, VCIN = 15V (Note-3)	—	—	0.01	mA	
	Ifo(L)		—	10	15		
Minimum Fault Output Pulse Width	tFO	VD = 15V (Note-3)	1.0	1.8	—	ms	

(Note-3) Fault output is given only when the internal SC, OT & UV protections schemes of either upper or lower arm device operate to protect it.

Mechanical Ratings and characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Mounting torque	—	Main terminal screw : M 5	2.5	3.0	3.5	N · m
Mounting torque	—	Mounting part screw : M 5	2.5	3.0	3.5	N · m
Weight	—	—	—	800	—	g

Recommended Conditions For Use

Item	Symbol	Condition	Recommended value	Unit
Supply Voltage	V_{CC}	Applied across P-N terminals	≤ 800	V
Control Supply Voltage	V_D	Applied between : $V_{UP1}-V_{UPC}$ $V_{VP1}-V_{VPC}$, $V_{WP1}-V_{WPC}$, $V_{N1}-V_{NC}$ (Note-4)	15.0 ± 1.5	V
Input ON Voltage	$V_{CIN(ON)}$	Applied between : U_P-V_{UPC} , V_P-V_{VPC} W_P-V_{WPC} , U_N-V_N , V_N-V_{NC}	≥ 0.8	V
Input OFF Voltage	$V_{CIN(OFF)}$		≥ 9.0	
PWM Input Frequency	f_{PWM}	Using Application Circuit of Fig.8	≤ 20	kHz
Arm Shoot-through Blocking Time	t_{dead}	For IPM's each input signals Fig.7	≥ 2.5	μs

(Note-4) With ripple satisfying the following conditions
 dv/dt swing $\leq \pm 5V/\mu s$, Variation $\leq 2V$ peak to peak

Precautions for testing

- Before applying any control supply voltage (V_D), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state. After this, the specified ON and OFF level setting for each input signal should be done.
- When performing "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
 (These test should not be done by using a curve tracer or its equivalent.)

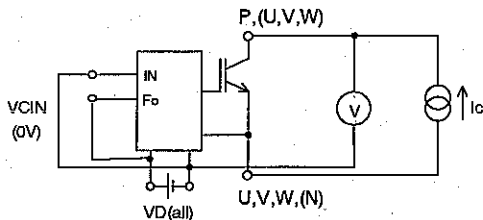


Fig.1 $V_{CE(sat)}$ Tset

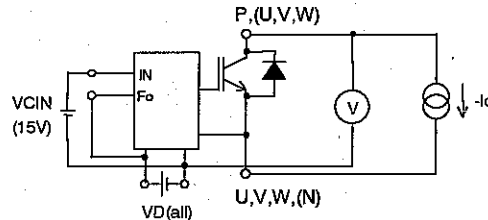


Fig.2 V_{EC} Tset

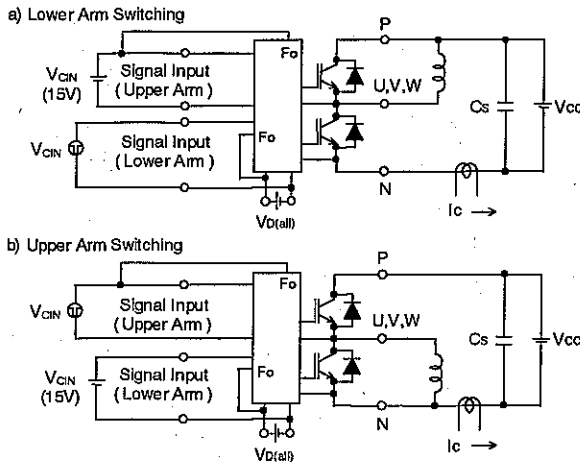


Fig.3 Switching time and SC test circuit

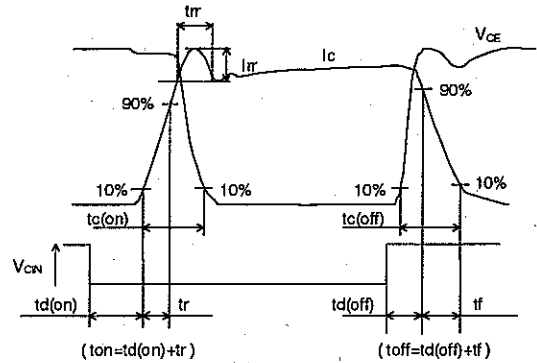


Fig.4 Switching time test waveform

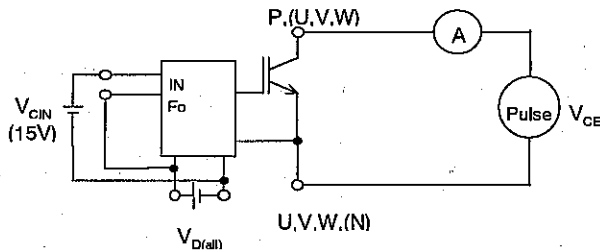


Fig.5 ICES Test

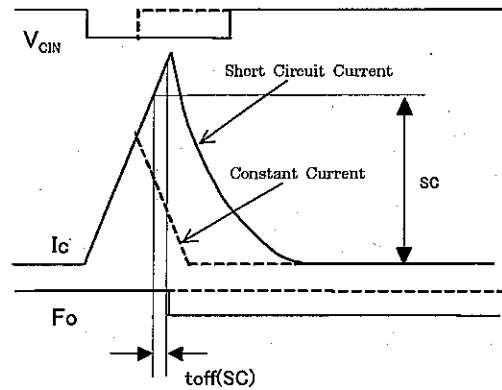
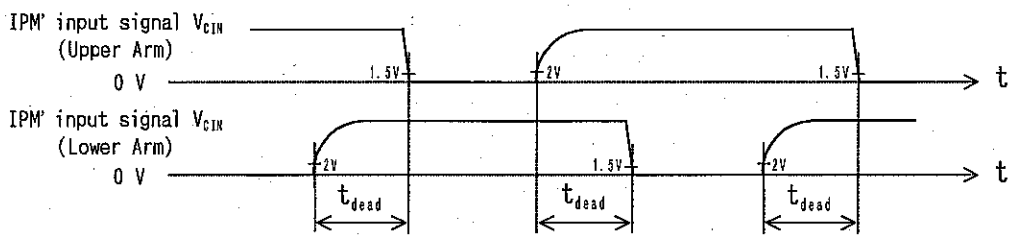


Fig.6 SC test waveform



1.5V: Input on threshold voltage $V_{th(on)}$ typical value, 2V: Input off threshold voltage $V_{th(off)}$ typical value

Fig.7 Dead time measurement point example

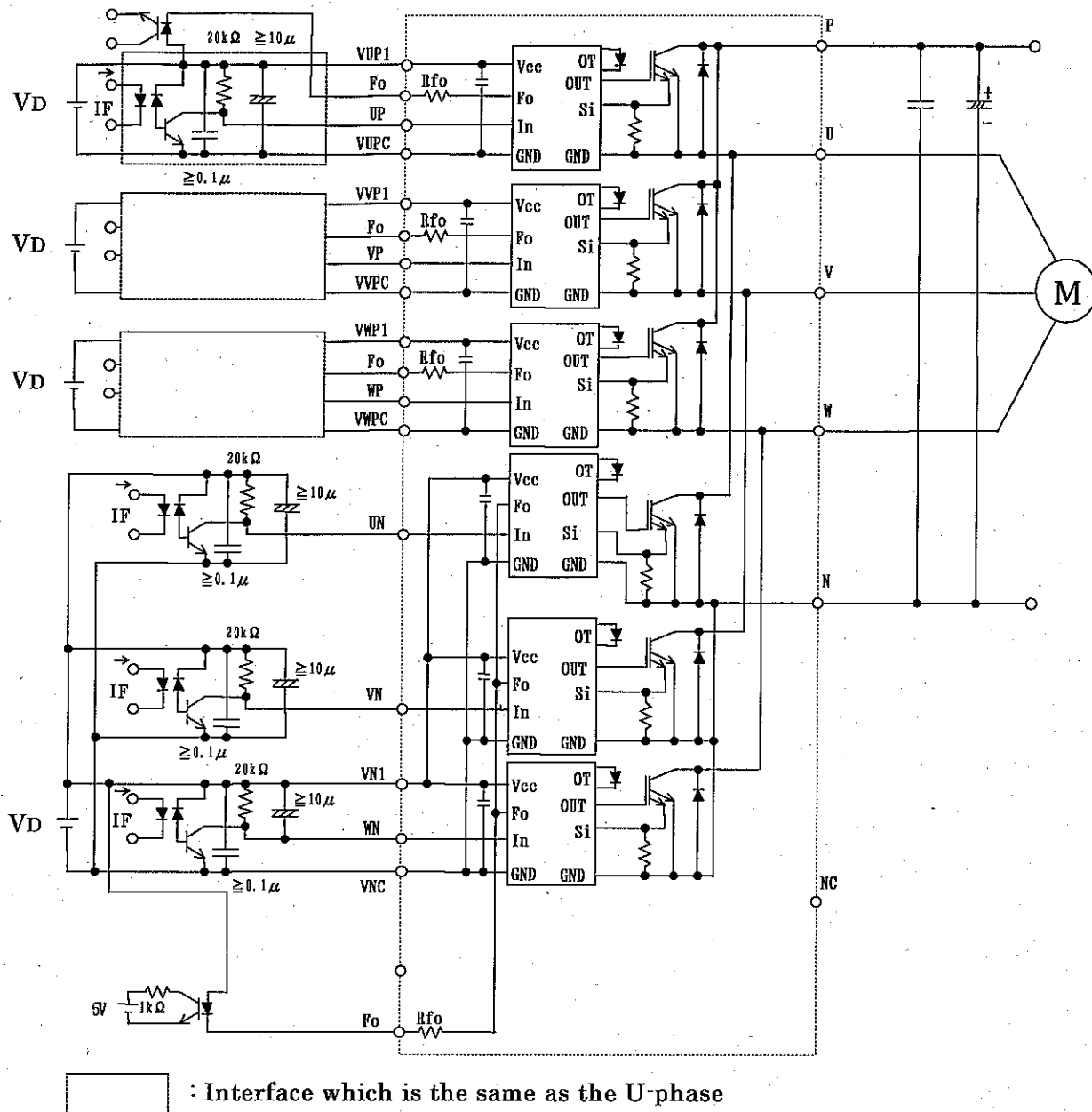


Fig. 8 Application Example Circuit

Notes for stable and safe operation ;

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers : $t_{PLH}, t_{PHL} \leq 0.8 \mu s$, Use High CMR type.
- Slow switching opto-coupler : $CTR > 100\%$
- Use 4 isolated control power supplies (V_D). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.

